ZUKEN

CADSTAR™

TOP FEATURES AND BENEFITS

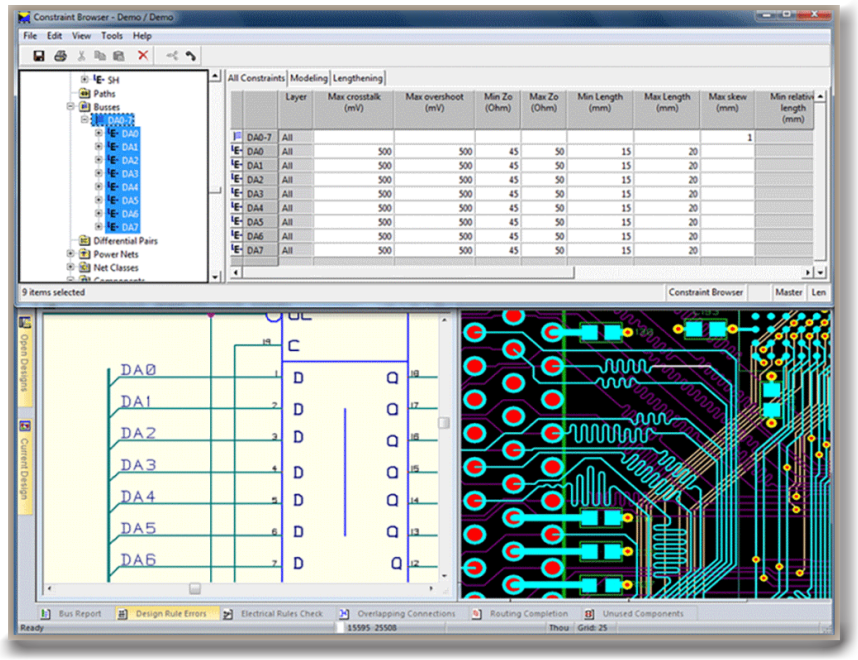
- Common constraint entry system for circuit design, layout, and analysis
- Assign standard or user defined topologies, such as H-Tree, Daisy Chain, or Star to control route order and timing for high-speed signals
- Automatic generation of extended nets, busses, and differential pairs
- Reduce constraint entry time with setup wizards for high-speed interfaces such as DDR2/DDR3 applications
- Spreadsheet interface to shorten learning curve and allow users to enter and confirm constraints in one view
- Export CSV and colored HTML reports to improve communication between design teams and to reduce effort in creation of documentation for validation
- Reuse constraints with CSV import to save time in constraint entry
- Support for hierarchical constraints to simply assignment of complex requirements between net classes

Constraint Management
CADSTAR Constraint Browser

Introduction

As design constraints increase in complexity, CADSTAR Constraint Browser simplifies constraint management by providing a fast and effective method to enter the most complex of rules. The Constraint Browser guides engineers through a fully integrated, constraints-driven design methodology to meet high-speed performance requirements, reducing design costs and time-to-market by eliminating unnecessary prototypes and re-engineering cycles.

The Constraint Browser provides an easy-to-use spreadsheet interface with constraint wizards to setup rules for applications, such as DDR2/DDR3 memory interfaces. The Constraint Browser works with CADSTAR Schematic to help you reduce your design cycle time and ensure that your designs are completed to the correct specifications.



Concurrent input and verification of high-speed constraints

The need for high-speed

Most digital applications require signals routed to a specification defined by a chip vendor to ensure effective signal quality and proper operation of the device. If you are working on adding an DDR2/DDR3 memory modules to your product, or dealing with multi-gigabit transceivers in your system, such as PCI Express, designers have to route signals to a set of constraints to meet specifications. With the Constraint Browser, engineers can capture these requirements early in the design process during circuit design and then verify and report the results at any time during layout and analysis.

Save time with automation

Constraint Browser simplifies constraint entry by automating the creation of high-speed objects in circuit design. If you have busses or extended-nets in your design, these objects are automatically extracted and available to access in the design tree view.

In today's world, high-speed designs can contain many differential pairs. Defining each one manually can be time consuming. In the Constraint Browser, you can define any combination of pairing rules based on the suffix or prefix of the positive and negative signal names. Differential pairs are automatically generated based on the pairing rules to save you time and effort towards managing your constraints.

Simplifying constraint entry

Constraint requirements are often complex and can be difficult to manage. To ease entry of constraints and provide flexibility for defining rules for any signal in a design, Constraint Browser supports multiple object levels and supports hierarchical constraints.

Engineers can define constraints for signals at the net, extended-net, and pin-pair level to help manage length control of each aspect of the signal. In cases where address and control lines propagate from a processor to several memory devices with series termination provided by a resistor array package, constraints can be set at each level to make certain that timing requirements are met within the skew tolerance. Constraints can also be set at the net class and design level for a hierarchy of constraints which allows designers to enter rules once for nets that share common values.

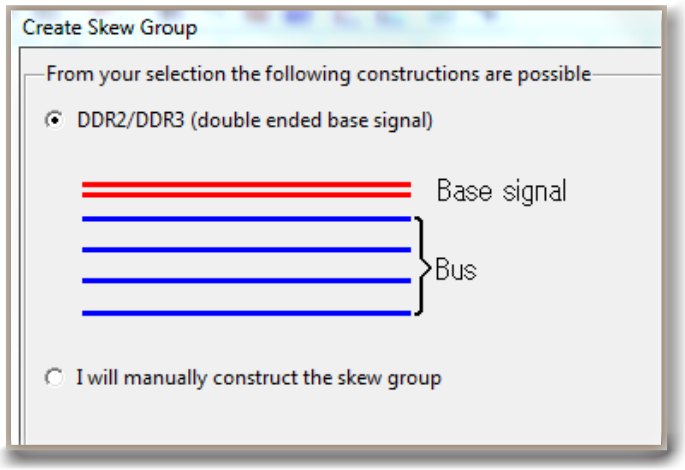
Topology planning

To achieve the desired timing requirements on high-speed nets, engineers must consider the proper pin order for routing. The Topology Editor in Constraint Browser provides engineers with a schematic view of the complete signal and options to control the pin order. Within the Topology Editor, engineers can assign a topology with predefined options, such as daisy chain, H-tree, or star topology, or create custom templates to apply to high-speed nets.

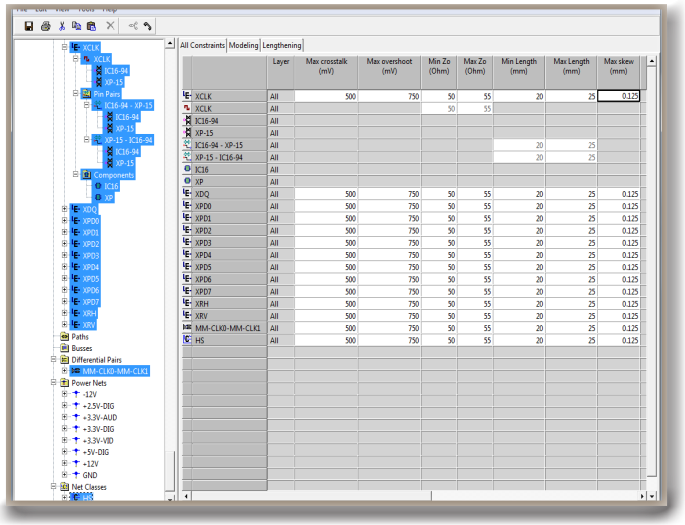
Documentation and constraint reuse

Constraint Browser supports import and export features to simplify documentation of a project and reuse of constraints between designs.

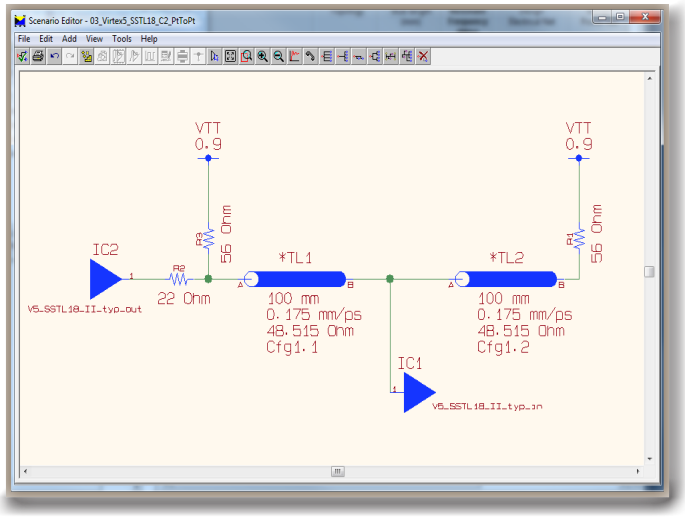
Engineers can create custom CSV and HTML reports to document settings and results of a project or to use them to communicate with other members of a design team. The CSV output can be modified and reused with the import function in Constraint Browser to save time and effort for the next design iteration or when a new project begins.



Skew group wizards for automatic setup of DDR2/DDR3 constraints



Set constraints for any object type in a design



Topology of a Virtex5 1.8V SSTL Class II termination