CADSTAR

CADSTAR FPGA (Active-HDL Lite) Installation & Licensing

CADSTAR Guide

SUMMARY

- CADSTAR FPGA software does not need to be installed in the CADSTAR software tree
- Aldec licensing setup is necessary, and is separate from CADSTAR FPGA licensing
- Registration of Aldec software is voluntary
- Standard VAR licences contain CADSTAR FPGA licences
- All three variants (VHDL, Verilog, Mixed) can be run
- CADSTAR FPGA can also be launched from within CADSTAR Design Editor

1. Installation

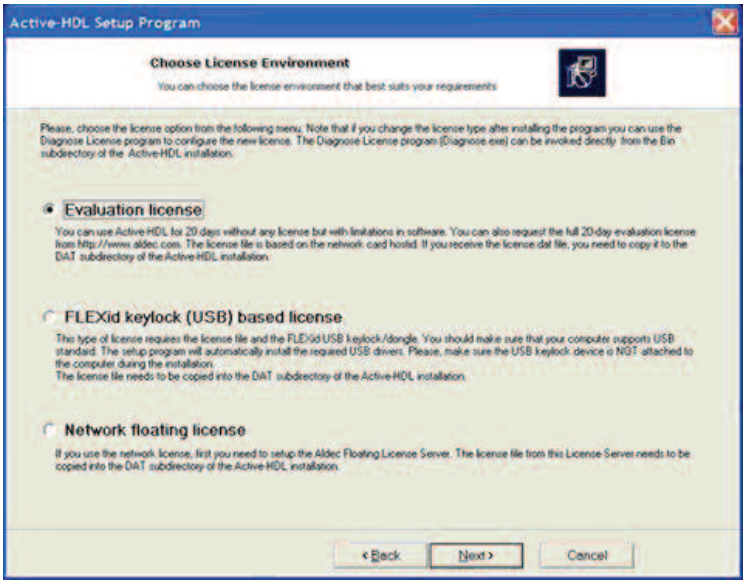
The CADSTAR FPGA (Active-HDL Lite) software should be obtained from the CADSTARworld website
http://www.zuken.com/cadstar/downloads.asp#CADSTARFPGA

This software can be used for evaluation purposes or for supplying software to fulfil a sales order. The software will run in the correct way depending on the authorisation (license file) used.

The CADSTAR FPGA software may be installed in the location preferred by the user – it does not need to be installed inside the CADSTAR software tree.

2. Licensing set-up during installation

As part of the software installation process for CADSTAR FPGA, an Aldec licensing setup dialog will be displayed (as shown in the screenshot below).



ZUKEN

This set-up is only for the Aldec licensing mechanism and does not affect the licensing of CADSTAR FPGA. **The CADSTAR FPGA licensing must be set-up separately after the software installation.** We recommend that you leave the *"Evaluation license"* option selected on this dialog and simply select *"Next>"* to continue with the installation. The correct licensing for CADSTAR FPGA will be set-up later.

At the end of the installation process there is a request to register the software and if this process is followed, you are taken to a registration page on the Aldec website (see image below):

This step is not necessary and the request to register can be safely ignored.

3. Licensing set-up

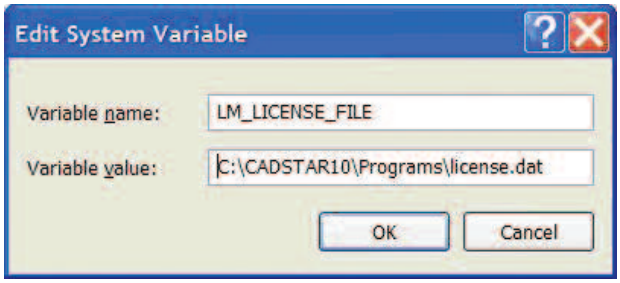
The licensing of CADSTAR FPGA is controlled and supplied by Zuken – not by Aldec. This will allow you to use the same dongle as used for CADSTAR itself and to have all licenses in the same, single license file.

The standard VAR license that you are supplied with each month will already contain the necessary licenses for CADSTAR FPGA – you do not need any additional licenses. The features provided in your VAR license will allow all three variants (VHDL, Verilog and Mixed) to be run. The appropriate features from the license file are as follows:

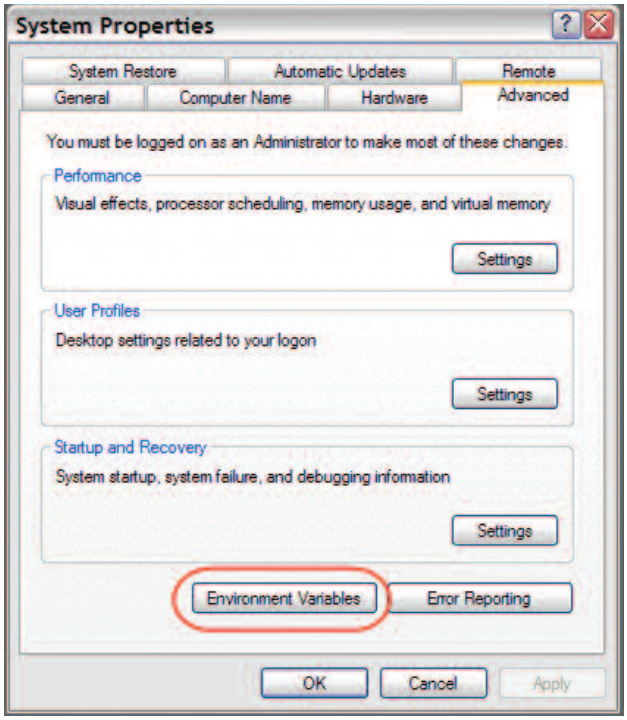
PACKAGE ADE_VLOG_LITE zuken 11.000 ...
PACKAGE ADE_VHDL_LITE zuken 11.000 ...
PACKAGE ADE_DL_LITE zuken 11.000 ...

To allow the CADSTAR FPGA software to locate the license file, you must first set the *LM_LICENSE_FILE* environment variable. This must be set to point to the location of the license file (the full path including the name of the license file).

So, if your VAR license is called *"license.dat"* and it is located in the *"Programs"* folder of the CADSTAR software installation (for example C:\CADSTAR10\Programs\license.dat), then *LM_LICENSE_FILE* needs to be set as in the following dialog:

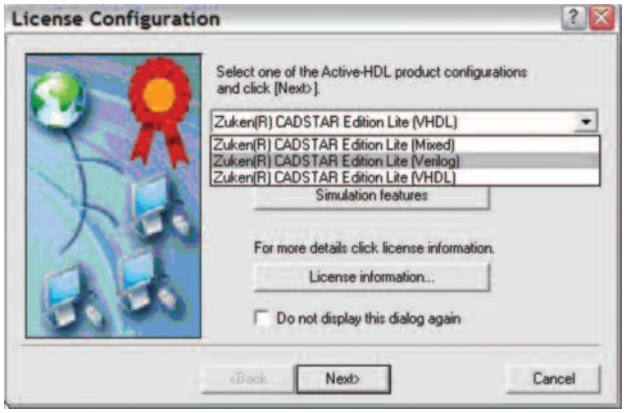


This dialog is accessed (on Windows XP) in the normal way, by right-clicking on *"My Computer"* and selecting *"Properties"* to display the System Properties dialog. On the *"Advanced"* tab, select *"Environment Variables"* and add a new System Variable as above.



Once *LM_LICENSE_FILE* has been set correctly, you will be able to run the CADSTAR FPGA software. From the Windows *"Start"* menu, the appropriate programs option to select is *"Active-HDL 7.3"*.

As the software runs up, it will display the following License Configuration dialog:



This will allow the product configuration which you wish to run to be selected (i.e. VHDL, Verilog or Mixed). This is the only option that needs to be selected from this dialog. Please ignore the *"License information…"* button. This only provides information on the Aldec licensing set-up which is NOT used at all by CADSTAR FPGA (Active-HDL Lite).

You may also launch the CADSTAR FPGA software directly from within the CADSTAR Design Editor (Schematic or PCB) from the *"Tools / Aldec Active-HDL"* menu option. However, for this menu option to be active/selectable, a valid component (marked as an FPGA part in the library) must first have been selected in the design.