ZUKEN®

CADSTAR™

CADSTAR Placement Planner

TOP FEATURES AND BENEFITS

- Define placement of critical components to optimize board performance and real estate early in the design process
- Engineers can manage schematic and layout reuse blocks to improve design cycle time
- Constraints and high-speed requirements are defined and tested before layout to reduce costly iterations
- View and cross-probe between schematic and PCB design data to ease verification
- Access to CADSTAR's many powerful placement features during schematic entry

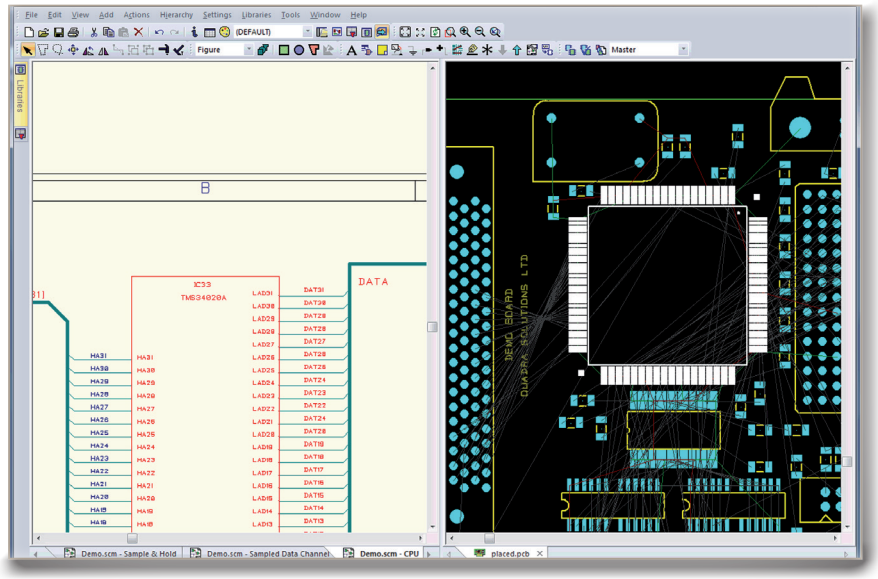
Introduction

CADSTAR Placement Planner enables the engineer to engage the placement process during logical circuit design. Whether you are conducting placement studies for real estate planning or defining the location of critical components, Placement Planner helps improve your design flow between logical design and PCB layout.

Placement Planner is an add-on to CADSTAR Schematics, and is intended to help electronic engineers communicate their intent and provide guidance to the PCB designer more effectively, without time-consuming iterations that can cause unnecessary delays.

Communication - Simplified

CADSTAR Placement Planner improves the communication link between the electrical engineer and PCB designer. In most design practices, once the logical design is completed, the engineer continues to utilize manual methods, such as paper or presentation slides to explain to a PCB designer the placement requirements of a design. Other communication methods include time spent in conference rooms or at a desk where the engineer will sit next to a PCB designer with the CAD system and define the most critical points for layout. These methods are time consuming. With Placement Planner, critical layout factors will be recognized and addressed early in the design process. CADSTAR Placement Planner promotes a tight working relationship between the electrical engineer and the PCB designer that will lead to a reduction in design time and improve design quality.



Place critical components with constraints

Design Reuse

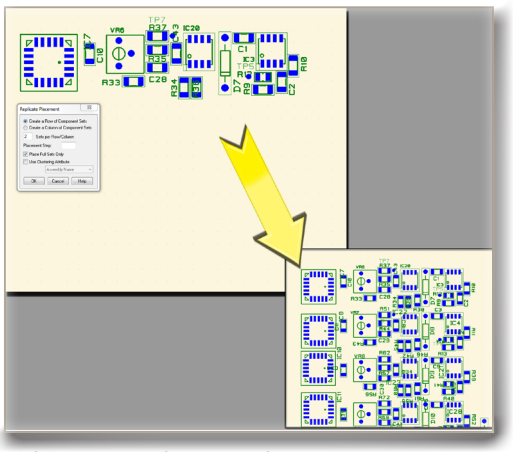
In the schematic, you can define sub-circuit blocks and use Placement Planner to start incorporating layout reuse blocks into the physical design. Reuse blocks can include parametric data, components, tracks, copper, and other artwork elements. This saves time and reduces rework by using known-good (or golden) circuits in the design. If the schematic contains replicated circuit blocks, then the engineer can use the multi-channel option to autoplace common circuits.

Constraint Management

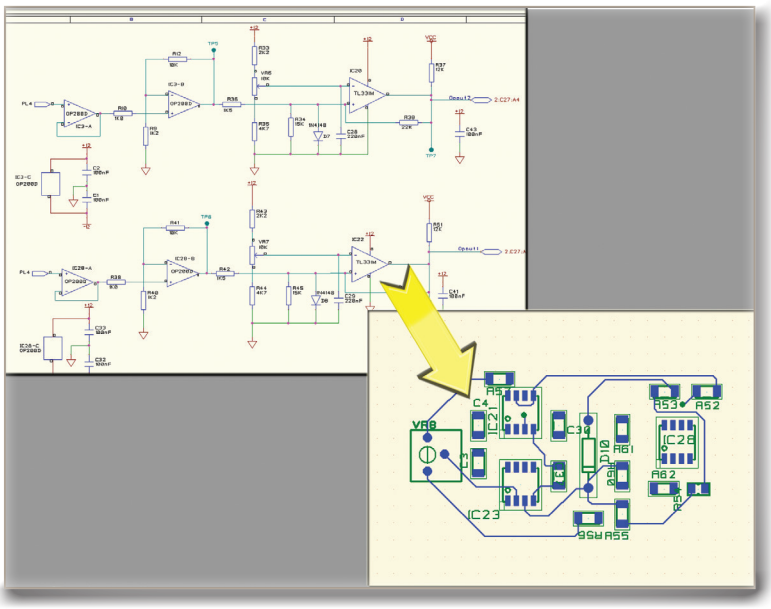
As technology and requirements continue to get more complex, the need to design with increasingly complex constraints has become more critical than ever. CADSTAR Placement Planner helps engineers ensure that the physical design conforms to the design constraints as defined in the schematic. Component placement is a key factor in meeting constraint requirements and, with Placement Planner, an engineer can test and optimize their placement early in the process using the many interactive and automated placement features within CADSTAR to insure that signal routing conforms to the constraints.

Managing Rules for High-Speed Design

Engineers can utilize Placement Planner to define layer combinations for various build-up technologies, ensure design rules meet manufacturing constraints, and manage complex spacing requirements. This allows you to define high-speed requirements early in the design process and, later, backannotate updates to the schematic. Placement Planner includes a spreadsheet-style table to help quickly define layer material specifications and generate views for scaled cross-section – essential for planning complex impedance profiles for high-speed designs.



Replicate common placement and routing

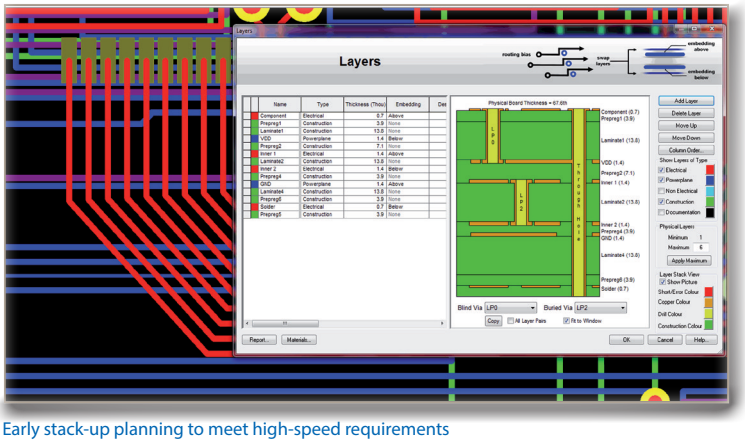


Assign reuse circuits and place layout reuse blocks

Beyond Placement

With the features of the CADSTAR Placement Planner at the engineer's fingertips, they can:

- Create board outlines with keep-in and keep-out rules
- Collaborate with mechanical engineers through import of DXF, IDF* and STEP* files (*IDF and STEP interfaces require additional licenses)
- Define copper areas
- Assign "StarPoints" for multiple ground plane interconnects
- Utilize the interactive and automated placement functions to ease component placement while obeying design rules
- Access the full library editor
- Conduct Engineering Change Order updates



Early stack-up planning to meet high-speed requirements